

**MODEL A6-CPS**  
Digital PLL  
**USER'S HANDBOOK**

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# 1 Safety Considerations

## 1.1 General

This product and related documentation must be reviewed for familiarisation before operation. If the equipment is used in a manner not specified by the manufacturer, the protection provided by the instrument may be impaired.

### 1.1.1 Before Applying Power

Verify that the product is set to match the available line voltage and the correct fuse is installed.

### 1.1.2 Before Cleaning

Disconnect the product from operating power before cleaning.

**WARNING**

**Bodily injury or death may result from failure to heed a warning. Do not proceed beyond a warning until the indicated conditions are fully understood and met.**

**CAUTION**

**Damage to equipment, or incorrect measurement data, may result from failure to heed a caution. Do not proceed beyond a caution until the indicated conditions are fully understood and met.**

### 1.1.3 This equipment must be earthed

An uninterruptible safety earth ground must be maintained from the mains power source to the product's ground circuitry.

**WARNING**

**When measuring power line signals, be extremely careful and use a step down isolation transformer whose output is compatible with the input measurement capabilities of this product. The product's front and rear panels are typically at earth ground. Thus, never try to measure AC power line signals without an isolation transformer.**

**WARNING**

**Instructions for adjustments when covers are removed and for servicing are for use by service-trained personnel only. To avoid dangerous electrical shock, do not perform such adjustments or servicing unless qualified to do so.**

**WARNING**

**Any interruption of the protective grounding conductor (inside or outside the instrument) or disconnecting of the protective earth terminal will cause a potential shock hazard that could result in personal injury. Grounding one conductor of a two conductor out-let is not sufficient protection.**

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If the instrument is to be energised via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earthed pole terminal (neutral) of the power source.

Instructions for adjustments while the covers are removed and for servicing are for use by service-trained personnel only. To avoid dangerous electrical shock, do not perform such adjustments or servicing unless qualified to do so.

For continued protections against fire, replace the line fuse(s) with fuses of the same current rating and type (for example, normal blow time delay). Do not use repaired fuses of short-circuited fuse holders.

## **1.2 Voltage, Frequency and Power Characteristics**

Voltage 14 – 30V DC (12 – 14V DC no on board OCXO)

Power characteristics 200mA Typical (50mA Typical no on board OCXO)

## **1.3 Environmental Conditions**

### **1.3.1 Temperature**

Operating (ambient) -10°C to +55°C (-65 to +65 op)

Storage -40°C to +85°C

## **1.4 Cleaning Instructions**

To ensure long and trouble operation, keep the unit free from dust and use care with liquids around the unit.

Be careful not to spill liquids onto the unit. If the unit does get wet, turn the power off immediately and let the unit dry completely before turning it on again.

Never spray cleaner directly onto the unit or let liquid run into any part of it. Never use harsh or caustic products to clean the unit.

## Digital PLL A6-CPS

### 2 Scope

The Quartzlock A6-CPS is a board level product designed for synchronising two stable oscillators. A typical example is the locking of a low phase noise OCXO to a rubidium frequency standard. The product uses a digital implementation of a standard phase lock loop.

## 3 Operating Procedure

### 3.1 Introduction

This module is designed to overcome the disadvantages of narrow band width analogue phase lock loops used to lock relatively stable oscillators together, or to generate arbitrary frequencies from a 10MHz reference with good phase noise, freedom from non-harmonically related spuri, and good short term stability.

When locking a low noise OCXO to a rubidium reference, for example, the ideal PLL bandwidth will be very much less than 1Hz, probably in the region of 10 to 100mHz. An analogue loop will have a very long time constant integrator, leading to thermal drift, capacitor dielectric absorption, and operational amplifier offset drift. In addition, acquisition time of the loop will be very long, and if there is any frequency error, acquisition may not occur at all. There is also a problem of providing an effective in lock indicator to the user, or for use with associated equipment.

The digital loop overcomes all these problems. The long time constant integrator is replaced by a digital integrator that does not drift at all. A combination of an analogue phase detector for low noise and an extended range phase/frequency detector for certain acquisition can be used. The loop bandwidth can be set to maximum for acquisition, followed by glitch free reduction to the working bandwidth when the phase error becomes small. In addition performance measures related to the phase error in the loop, and the frequency error can easily be derived and used to indicate lock and bandwidth control. As an additional benefit a hold over mode that keeps the controlled oscillator tuning voltage constant if there should be a reference failure can be easily provided.

In order to generate arbitrary frequencies from a 10MHz reference, a DDS synthesiser is used. This has 36 bit resolution and is clocked at 10MHz from the reference. Output frequencies of 1.8MHz to 3.6MHz are available as the reference input to the digital PLL. This enables the controlled oscillator (OCXO) to have a frequency range of 1.8MHz to 28.8MHz. The resolution at 10MHz output will be  $1.45 \times 10^{-11}$ .

### 3.2 Technical details of design

The design uses switching mixer type phase detectors operating at frequencies between 1.8MHz and 10MHz. A dual phase detector is used with quadrature square wave inputs from the controlled oscillator. The main input, which is split between the quadrature phase detectors, is a sine wave input at a level between 0 and 13dBm, and is link selected to either come from the 10MHz reference input, the output of the DDS synthesiser, or the reference divided by 2.

The sine wave signal from the controlled oscillator is converted to a square wave using a fast comparator. It is then divided by 2, 4 or 8 using digital dividers. A link selects direct, 2, 4, or 8 divided signals.

The output from the dividers forms the "Q" reference signal to the Q phase detector. A quadrature "I" reference is generated by passing the Q signal through a programmable delay line, which may be set to delays from 10ns to 137ns, in steps of 0.5ns. This enables quadrature references to be generated for phase detector frequencies between 1.8MHz and 25MHz.

The outputs from the phase detectors are filtered and amplified by DC amplifiers with gain control using digital potentiometers. The gain is controlled by a software AGC system which tries to keep the input to the ADCs at optimum levels. The phase detector outputs are sampled by two channels of the 10bit A to D convertor internal to the PIC 16F689 microcontroller. All other functions of the PLL are carried out by software.

The control of the OCXO or other controlled oscillator uses a precision tuning voltage derived from D to A convertors. Two 16 bit DACs are used, with the output of the fine tune DAC divided by 256 and added to the output of the coarse tune DAC. This gives effectively 24 bit resolution with an overlap between the coarse and fine tune DACs. A software normalisation process ensures that the fine tune DAC is used for tuning most of the time. Only when the controlled oscillator has drifted out of range of the fine tune DAC would the coarse tune DAC need adjusting, with the chance of a very small glitch in the tuning voltage. A precision, low noise, voltage reference is used to supply the DACs.

The microcontroller is provided with an RS232 interface. A simple set of control codes enable monitoring and set up of the digital PLL parameters to accommodate a wide range of controlled oscillators. A Windows front end program will use the control codes to enable the operation of the PLL to be monitored with real time graphs of performance measures.

See Appendix B for Block Diagram.

### 3.3 Software design

The input to the software is the sampled I and Q signals from the phase detectors. These are sampled at a 1kHz rate. As the final bandwidth of the PLL will be less than 1Hz, this oversampling enables pre-filtering to be used which extends the resolution and reduces noise in the 10bit A to D convertor internal to the microcontroller. Single pole digital filters are used on both the I and Q channels. These are implemented as exponential filters which have a 3dB band width which is a function of the "order" of the filter. Filter orders between 0 (no filter) and 15 are provided. This gives bandwidths

between 114Hz for order 1, and 4.8mHz for order 15. The filter order is varied as the user selected PLL bandwidth is varied.

After pre-filtering, the I and Q channels, now at 16 bit resolution, are sub-sampled at a rate between 15.625 s/s, and 1.953 s/s depending on the user bandwidth and lock state of the PLL. The "Q" sample is now divided by the "I" sample (after checking that I>Q) to give a binary fraction. This is used to look up the phase value in a TAN-1 look up table. The look up table is used to synthesise 2 types of phase detector:

- a. A phase detector with 16 bit resolution between  $\pi/2$  and  $-\pi/2$ .
- b. A phase/frequency detector with 16 bit resolution between  $2\pi$  and  $-2\pi$ . This phase detector is equivalent to the well known digital phase/frequency detector. This rolls over between  $2\pi$  and 0 for positive cycle slips, and between  $-2\pi$  and 0 for negative cycle slips, and will always provide reliable lock if there is a initial frequency error.

The output of the selected phase detector now has digital gain applied, selectable between 1/256 and 128. After digital gain, the phase value is added into the integrator, which is 32 bits wide.

In order to make the loop stable, by providing a phase lead, the phase value has proportional term gain applied, also selectable between 1/256 and 128. This value is added to the upper 3 bytes of the integrator to give the tuning voltage (24 bits)

The tuning voltage is divided between the coarse and fine tune DACs as follows: When normalisation is performed, the fine tune DAC most significant 8 bits are set to mid point (80h). The least significant 8 bits of the fine tune DAC are set to the least significant 8 bits of the tuning word. The coarse tune DAC is then set to provide the final tuning voltage. During all subsequent tuning, only the fine tune DAC is used over its 16 bit range. If the range is exceeded, the normalisation procedure is repeated.

A state machine provides control of locking. After reset the last value of the integrator, which has been stored in EEPROM on a regular basis, is restored. This will retune the controlled oscillator to very nearly the correct frequency. The loop is then opened and the software waits for the following all to occur (state 0):

- a. Rubidium reference warm up input to go high.
- b. OCXO supply current to drop below a threshold showing the OCXO has warmed up
- c. A measure  $|I+|Q|$  which is an approximate measure of the signal level at the phase detector to rise above a threshold.

When these conditions are fulfilled, the software attempts to lock the loop (state 1) by selecting the phase frequency detector, maximum bandwidth, and maximum subsample rate. It then closes the loop and waits for another measure, which is  $|\text{phaseresult}|$  (delta phi in the block diagram), to drop below a threshold. The measure  $|\text{phaseresult}|$  is the modulus of each phase calculation filtered in an 8th order exponential filter, the bandwidth of which, for the 15.625 s/s subsample rate, equals 9.7mHz.

Once the lock threshold for  $|\text{phaseresult}|$  is reached, the lock state (state 2) is entered. The bandwidth is switched to the users selected bandwidth, which has been maintained in EEPROM, and the phase detector is switched over to the narrow band phase detector ( $\pi/2$  to  $-\pi/2$ ). All the time during normal operation,  $|\text{phaseresult}|$  is being compared to a lower threshold than the lock threshold. If it exceeds this threshold, state 3 is entered which provides a brief flash of the lock LED to warn the user that the selected bandwidth may be too narrow for the PLL to track the drift of the controlled oscillator fast enough. This low threshold is currently set at 480ps maximum phase error (at 10MHz phase detector frequency).

In extreme cases the lock threshold (4.8ns phase error) may be exceeded, in which case the software assumes lock is lost and re-enters state 1.

A further performance measure is calculated, which is available over the interface. This is the first difference of the phase error, filtered in an 8th order exponential filter. It is corrected for subsample rate, and has a constant sensitivity of  $5.8 \times 10^{-15}$  per bit. (at 10MHz phase detector frequency)

This performance measure gives the mean fractional frequency difference between the controlled oscillator and the reference, and is useful for setting up the optimum bandwidth of the PLL.

The band width and damping of the PLL is controlled by 4 parameters, integrator digital gain, proportional digital gain, pre-filter order, and subsample rate. These are preset for 8 values of user selected bandwidth, and can only be changed by modifying the software. It is possible to temporarily adjust the four individual parameters as part of a test procedure carried out over the RS232 interface. The selection of the 4 parameters has been optimised using a mathematical model

of the PLL modelled as a MATHCAD spreadsheet. This could be made available to customers who wished to readjust the PLL parameters.

### 3.4 Interface

The RS232 interface enables setup and monitoring of the DPLL.

The basic control codes are defined in appendix A. The purpose and operation of the control codes are considered in this section.

#### 3.4.1 Basic

All control codes operate on fixed string lengths, there is no terminator character, i.e. "enter" is not required.

All control codes start with two letters (upper case only) which defines the control group. In each group the code may be followed by a "?", a "+" or an additional letter (upper case) with a variable length hexadecimal string. In a few cases only the initial two letters are required, in which case the microcontroller will acknowledge with a single carriage return character (0Dh) after the initial two characters.

The "?" as the third character (query command) will return a hex string representing the current setting of the parameters appropriate to the control group, followed by a carriage return.

The "+" as the third character will enter the query command into the internal repeat stack. The command will then be repeatedly processed at a preset rate. The operation of the command repeat facility is described later.

The control groups which accept an additional letter are intended to update internal parameters, and are described fully under each control group. After updating a parameter, the controller will reply with a carriage return and an automatic repeat of the query form of the control group.

If an invalid code or string is sent that cannot be parsed, the controller will reply with "!" "carriage return", and will clear the input buffer.

#### 3.4.2 Detailed use of interface commands.

##### **WARNING**

**By incorrect use of the interface, it is possible to get the controller into a state where the PLL will not work. The key command to avoid is "EU" (EPROM update) which writes any changed parameters into the EPROM memory. Provided this is not done, a power on reset will always restore the previous values. An alternative to the power on reset is the command "SR" (software reset).**

#### 3.4.3 Command list

##### **UA (user adjust)**

This command is intended for the user to change the PLL control bandwidth. The command "UA?" returns a string of 1 byte, followed by 2 bytes.

The first byte is the PLL bandwidth, range 0 to 7, with 0 the minimum bandwidth. bits 3 to 7 of the byte are not used.

The second pair of bytes is the power on time of the microcontroller since the firmware was programmed. This is in units of 2.33 hours. This parameter cannot be changed using the interface. (but see "ER" command).

To change the bandwidth, send "UABxx" where xx is the new bandwidth byte.

After changing the bandwidth, the command "EU" must be used to update the EPROM with the new bandwidth.

The actual physical control bandwidth of the PLL will depend upon the tuning sensitivity of the OCXO or other controlled oscillator, also the division ratio between the controlled oscillator and the phase detector. In a later section hints will be given for configuring the board for a new application, which will include aspects of the PLL control parameters.

##### **OS (overall status)**

This command monitors and controls the state machine which controls the locking and monitoring of the PLL. It also controls various test modes which are more concerned with product development than user adjustment. However there are two functions which need to be set up using this command for a new application. These are the delay line setting, and the tuning voltage span.



"OS?" returns 8 hex strings of different lengths. The control code definition section has a full specification of these.

#### ***Test status byte***

The test status byte switches on and off various functions for test purposes. To change a particular bit, a new hex string must be calculated. One of the most important bit switches is bit 7, which when set disables the automatic lock control state machine, and enables the PLL to be manually controlled. In order to open the control loop, set bits 3 and 4.

Bits 0, 1, 2 control the special use of the fine tune DAC. This can be set to output any of the listed internal parameters at a sample rate of 2ks/s. The most useful is the phase result. Display of this parameter on an oscilloscope will show the loop pulling in and locking. When using the fine tune DAC for test purposes, link JP1 should be opened to disconnect the fine tune DAC from the tuning voltage, as otherwise strange results may be observed. The PLL will work quite well with just the coarse tune DAC used for tuning.

**IMPORTANT** The test status byte is maintained in EPROM. If the command EU (EPROM update) is used when the test status byte has been manually altered, the unit may not work after the next power on reset. If in doubt, the test status byte should be set to 00hex, and the EU command executed.

#### ***Lock status byte***

The lock status byte monitors the operation of the state machine. Bits 0, 1, 2 indicate the current internal state. Bits 4, 5 are read only bits which indicate the state of the OCXO and PLL. Bits 6, 7 are automatically controlled by the state machine, but may be set and reset by the user for test purposes. In order to avoid overwrite by the state machine; bit 7 of test status should be set.

Bit 6 switches between the narrow range high sensitivity phase detector (range  $\pm\pi/2$ , resolution 16 bits) and the wide range low sensitivity phase/frequency detector (range  $\pm 2\pi$ , resolution 16bits)

Bit 7 prevents the use of the user preset PLL bandwidth. Every time the PLL algorithm is run, which occurs at the subsample rate, the user bandwidth parameter (0 to 7) is used to look up a table which contains the 4 parameters that control the dynamic behaviour of the loop. These are subsample rate, exponential filter order, integrator gain, and proportional gain. When the loop is unlocked, the state machine sets this bit to inhibit the update. It then loads special parameters which are only used during locking. This gives the loop maximum bandwidth and an under damped response which provides the fastest possible frequency and phase pull in.

#### ***PLL control (2 bytes)***

These bytes contain the current PLL parameters. These will be refreshed continually from the look up table unless bit 7 of lock status is set. These parameters may be varied by the user; however they are not stored in EPROM memory. The look up table which relates the user bandwidth parameter to the PLL control parameters is stored as a lookup table in program memory, and can only be changed by reloading the firmware.

#### ***Quadrature delay line setting (1 byte)***

This user adjustable parameter controls the delay setting of the digital delay line that provides the "I" input to the phase detectors. The delay required depends upon the comparison frequency at the phase detectors. For 10MHz comparison, the required delay is 25ns. The delay line has a fixed delay of about 10ns, and a variable delay of about 0.5ns per bit. Thus to obtain 25ns total delay, the setting is 30 decimal or 1Eh. The approximate setting can be calculated from the comparison frequency using the above example. Later in this manual a procedure for accurate setting of the delay will be given

The delay parameter should be stored in EPROM after change, using the "EU" command.

#### ***Tune voltage span (1 byte)***

The tune voltage span can be set to suit the OCXO. A value of 00h will give a span of 0 to 10V, and a setting of FFh a span of 0 to 5.8V.

After setting the value should be stored in EPROM using the "EU" command.

#### ***Q amp AGC setting.***

The AGC system tries to optimise the variable gain amplifiers that follow the phase detectors so the input ADCs operate over their full range. As the normal lock point is with the Q channel near the midpoint of the ADC range (2.5V), the I channel actually controls the AGC level when the loop is locked. When unlocked there is a sine wave at both the I and Q channels so both ADCs will control the AGC.

There is little point in the user controlling the amplifier gains manually, although this is possible by writing to these bytes. Bit 5 of test status must be set first.

#### ***I amp AGC setting***

See previous description

**OCXO current (2 bytes).**

These bytes are read only and give the filtered value of the OCXO supply current. The range is 0 to 500mA. The digital filter has a 3dB bandwidth of about 5mHz, so the value responds quite slowly to a change in OCXO current. The value is compared to a threshold to detect OCXO warm up. When the current falls below the threshold, the state machine will move to state 1 and try and lock the loop. The OCXO threshold is not adjustable without reloading the firmware.

**PL (phase lock loop)**

This command monitors the current state of the PLL. It also enables user adjustment of some of the parameters.

Last value of I sample (filtered), 2s complement, 16 bit (2 bytes)

This is the output of the pre-filter (exponential filter) on the I phase detector channel. It is a signed integer in 2s complement format.

Last value of Q sample (filtered), 2s complement 16 bit. (2 bytes)

ditto Q channel

Last value of PLL integrator, 32 bit integer (4 bytes).

Current value of the integrator. This may be overwritten with the PLI command. This is useful for transient testing of the PLL response as it represents a step in the tune voltage.

Coarse tune DAC, 16 bit integer

Fine tune DAC, 16bit integer

Current value of the coarse and fine tune DACs. In normal operation the tuning DACs are updated at the subsample rate. If bits 3 and 4 of the test status byte are set, i.e. there is no integrator update or proportional term, and then the update of the tuning DACs is inhibited. In this situation the DACs may be written to with the PLC and PLF commands.

**PD (phase detector)**

This command outputs various measures associated with the phase calculation.

Last phase result, 16bit 2s complement, 2 bytes

This useful measure shows the current phase error after the phase calculation. This is after the pre-filtering of the I and Q samples. The phase calculation occurs at the subsample rate.

Last mod(I) + mod(Q) 16bit integer

This is the filtered value of mod(I) +mod(Q). This is the approximate magnitude of the signal after the I and Q ADCs

2.5V reference

This is the filtered result of converting the reference channel of the ADC

mod(phase result) (filtered)

This important measure is the filtered magnitude of the phase error. It is the main measure that the software uses to determine if the loop is in lock. If this measure is greater than a threshold, the lock LED will flash. If the measure increases above a second threshold, the lock state machine will assume that lock has been lost, and will switch to state 0 to try and re-establish lock.

mod(freq offset) (filtered)

## 4 Specification

### REFERENCE INPUT

FREQUENCY:	10MHz 1MHz to 10MHz	(DDS is used) (No DDS)
LEVEL:	100mV PP to 5VPP 1VPP to 5VPP	(DDS is used, REF/2 is used) (No DDS)
INPUT IMPEDANCE:	1000 OHMs	

### CONTROLLED OSCILLATOR

FREQUENCY:	1MHz to 40MHz 1.8MHz to 28.8MHz	(DDS not used) (DDS is used)
LEVEL (external oscillator)	100mVPP to 5VPP	
INPUT IMPEDANCE	500 Ohms	

EXTERNAL TUNE VOLTAGE 0 to SPAN, where SPAN is software adjustable between 5.8V and 10V

### Notes:

- If DDS is not used, controlled oscillator must be k/m times higher frequency than reference, where k is link adjusted to 1,2,4,8., and m is link adjusted to 1 or 2. m is reference divider.
- Either reference or controlled oscillator must be 10MHz to provide microcontroller clock

POWER SUPPLY:	14 to 30V 12 to 30V	(on board OCXO is used) (no on board OCXO)
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CURRENT CONSUMPTION:	150mA typical 50mA typical	(on board OCXO) (no on board OCXO)
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PLL BANDWIDTHS 4mHz to 500mHz typical in 8 binary increments

FREQUENCY PULL IN up to 7Hz initial frequency error

LOCK INDICATOR	on off short flash every second: long flash, short flash	not locked locked, low phase error locked, high phase error no processor clock
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INTERFACE 9.6kbaud, RS232, PC compatible

INTERFACE CODES see separate document

## 5 Appendix A

RS232 control codes (all values following command or returned from the microcontroller are hexadecimal)

\* = backed up in EEPROM

### UA User adjust

UA? returns user parameters

*aa bbbb*

*aa* is bandwidth control: bits set: bit 0,1, 2: bandwidth ( 0 to 7)  
bit 3: set to inhibit auto load of PLL gain parameters

\* *bbbb* is clock registers 3 and 4 ( elapsed time)

UABaa write new bandwidth control byte

### OS Overall Status

OS? returns overall status bytes:

*aa bb cccc dd ee ff gg hhhh*

*aa* is test status byte: bits set:: bit0,1,2: bits 0 to 2 DAC output select  
bit3: no integrator update  
bit4: no proportional term  
bit5: AGC off  
bit6:  
bit7:  
*bits 2,1,0: 000 no test output, fine tune DAC used for tuning*  
*001 sub sampled I*  
*010 sub sampled Q*  
*011 PLL Integrator upper 16 bits*  
*100 Phase result*  
*101 I sample (filtered)*  
*110 Q sample (filtered)*  
*111 reference CH6 (filtered)*

*bb* is lock status byte: bits set bit0 to 2: State control, states 0 to 7  
bit3: set to normalise tuning DACs (cleared automatically)  
bit4: OCXO warmed up  
bit5: Loop locked  
bit6: narrow range phase detector in use  
bit7: set to inhibit state control

*cccc* is PLL control: bits set bit0,1,2,3 subsample rate  
bit4,5,6,7 exp filter order  
bit8,9,10,11 integrator gain  
bit12,13,14,15 proportional gain

\* *dd* is quadrature delay line setting

\* *ee* is tune voltage span (FFh min,00h max) 0 to 5.8V ( FFh), and 0 to 10V (00h):

*ff* is Q amp AGC setting

*gg* is I amp AGC setting

*hhhh* is OCXO current

OSTaa write new test status byte

OSLbb write new lock status byte

OSGcccc Write new PLL control

OSDdd Write new quadrature setting

OSSee Write new tuning span

OSQff Write new Q amp AGC byte

	OSIgg	Write new I amp AGC byte
<b>PL</b>	<b>Phase lock loop</b>	
	PL?	returns current status of PLL
		<i>aaaa bbbb ccccccc dddd eeee</i>
	<i>aaaa</i>	<i>last value of I sample(filtered) , 2s complement, 16 bit</i>
	<i>bbbb</i>	<i>last value of Q sample(filtered), 2s complement 16 bit</i>
*	<i>ccccccc</i>	<i>last value of PLL integrator (32 bit integer)</i>
	<i>dddd</i>	<i>Coarse tune DAC 16 bit integer</i>
	<i>eeee</i>	<i>Fine tune DAC 16 bit integer</i>
	PLccccccc	write new PLL integrator
	PLCdddd	write new coarse tune DAC
	PLFeeee	write new fine tune DAC
	PL+	enter command PL? into repeat stack
<b>PD</b>	<b>Phase detector</b>	
	PD?	returns phase detector parameters
		<i>aaaa bbbb cccc dddd eeee</i>
	<i>aaaa</i>	<i>Last phase result, 2s complement</i>
	<i>bbbb</i>	<i>Last mod[I] +mod[Q]</i>
	<i>cccc</i>	<i>2.5V reference (filtered)</i>
	<i>dddd</i>	<i>mod (phase result) (filtered) lsb=0.763ps</i>
	<i>eeee</i>	<i>mod(freq offset) (filtered) lsb = 5.82E-15</i>
	PD+	write PD? to command repeat stack
<b>EU</b>	<b>EEPROM update (backed up values)</b>	
<b>SR</b>	<b>Software Reset</b>	
<b>ER</b>	<b>EEPROM read</b>	
	ERCaabb	returns bb bytes from starting address aa as ASCII characters
	ERNaabb	returns bb bytes from starting address aa as hexadecimal numbers (character pairs)
<b>EW</b>	<b>EEPROM write</b>	
	EWCaabbcccc-----c	
		writes bb characters to starting address aa. Correct number of characters must be included in string
	EWNaabbcccc-----c	
		Writes bb bytes to starting address aa. Character pairs cc etc are interpreted as hexadecimal numbers.
<b>RI</b>	<b>Repeat Interval</b>	
	RI?	returns command repeat interval
		<i>aa</i>
	<i>aa</i>	<i>8 bit command repeat interval multiplier. Range 1 to 255. Command repeat interval is 50ms x aa</i>
	RI0aa	write new command repeat interval
	RID	cancel command repeat and clear command repeat stack

6 Appendix B



